REQUEST FOR ACTION (RFA) RESPONSE

GLAST LAT Project
Calorimeter Peer Review **17 – 18 March 2003**

Action Item:	CAL – 015
Presentation Section:	Thermal
Submitted by:	Tom McCarthy

Request: Thermal analysis – Board -Add list of derated part temperatures that apply to all parts as part of the Board level temperature summary.

Reason / Comment: The board level thermal analysis needs to show that the thermal design of the board/box maintains part temperature below derated limits in the Qual environment.

Response:

The attached view graph corrects the board level thermal analysis summary that was presented at the Peer Review to address the request of this RFA.

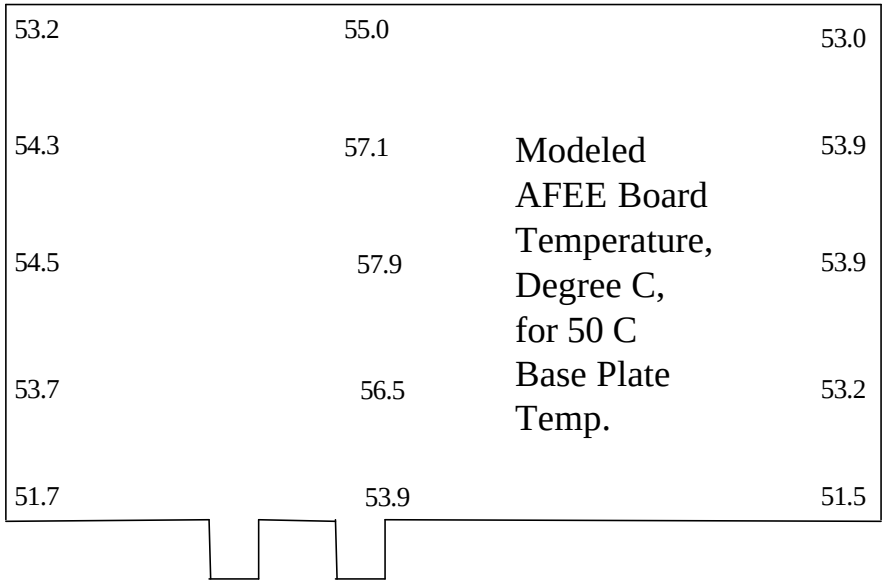
The AFEE Thermal Study report will be updated to add this information. It can be found via URL:
http://hese.nrl.navy.mil/glast/CM/rpt/AFEEThermalStudy-LAT-TD-01114-02.pdf

AFEE Thermal Analysis

- **AFEE Thermal Analysis Summary.** From LAT-TD-01114-01 Dated 4/03
  Author Peck Sohn, Swales Aerospace
- **Maximum silicon die temperatures for 50 C Qual Base Plate temperature**

Device	GCRC	GCFE	ADC	DAC	Ref.
Modeled Die Junction Temp. Deg. C	61.3	58.2	58.5	58.4	59.7
Maximum Derated Die Temperature, Deg. C	93	93	93	93	93

- **Analysis result, Calorimeter AFEE electronics do not have any thermal problems**



Assumptions

	Modeled Heat Dissipation	Theta Junction to Board (C/W)
GCRC	65 mW	50
GCFE	11.5 mW	114
ADC	2 mW	183
DAC	4 mW	86
Ref.	7 mW	232
Total Power per AFEE	952 mW	
AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers.		